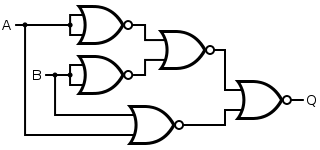
Develop neuron and print truth table of XOR gate using only NOR gates



=( (A NOR A) NOR (B NOR B)) NOR (A NOR B)

|  |  |  |
| --- | --- | --- |
| A | A | Q1 |
| 0 | 0 | 1 |
| 0 | 0 | 1 |
| 1 | 1 | 0 |
| 1 | 1 | 0 |

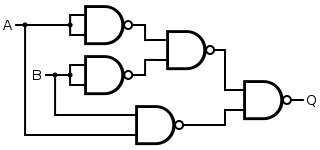
|  |  |  |
| --- | --- | --- |
| B | B | Q2 |
| 1 | 1 | 0 |
| 0 | 0 | 1 |
| 0 | 0 | 1 |
| 1 | 1 | 0 |

|  |  |  |
| --- | --- | --- |
| Q1 | Q2 | Q3 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |
| 0 | 1 | 0 |
| 0 | 0 | 1 |

|  |  |  |
| --- | --- | --- |
| A | B | Q4 |
| 0 | 1 | 0 |
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

|  |  |  |
| --- | --- | --- |
| Q3 | Q4 | Q |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 0 | 0 | 1 |
| 1 | 0 | 0 |

Develop neuron and print truth table of XNOR gate using only NAND gates



= [ ( **A** NAND **A** ) NAND ( **B** NAND **B** ) ] NAND ( **A** NAND **B** )

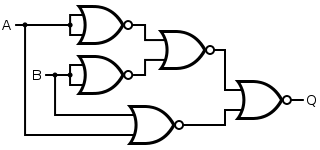
|  |  |  |
| --- | --- | --- |
| A | B | Q1 |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |
| 1 | 0 | 1 |

|  |  |  |
| --- | --- | --- |
| A | A | Q2 |
| 0 | 0 | 1 |
| 0 | 0 | 1 |
| 1 | 1 | 0 |
| 1 | 1 | 0 |

|  |  |  |
| --- | --- | --- |
| B | B | Q3 |
| 0 | 0 | 1 |
| 1 | 1 | 0 |
| 1 | 1 | 0 |
| 0 | 0 | 1 |

|  |  |  |
| --- | --- | --- |
| Q2 | Q3 | Q4 |
| 1 | 1 | 0 |
| 1 | 0 | 1 |
| 0 | 0 | 1 |
| 0 | 1 | 1 |

|  |  |  |
| --- | --- | --- |
| Q1 | Q4 | Q |
| 1 | 0 | 1 |
| 1 | 1 | 0 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

- Develop neuron and print truth table of XNOR gate using only NOR gates

=((A NOR A) NOR (B NOR B)) NOR (A NOR B)

|  |  |  |
| --- | --- | --- |
| A | B | Q1 |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 1 | 0 |
| 1 | 0 | 0 |

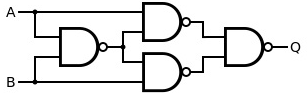
|  |  |  |
| --- | --- | --- |
| A | A | Q2 |
| 0 | 0 | 1 |
| 0 | 0 | 1 |
| 1 | 1 | 0 |
| 1 | 1 | 0 |

|  |  |  |
| --- | --- | --- |
| B | B | Q3 |
| 0 | 0 | 1 |
| 1 | 1 | 1 |
| 1 | 1 | 0 |
| 0 | 0 | 1 |

|  |  |  |
| --- | --- | --- |
| Q2 | Q3 | Q4 |
| 1 | 1 | 0 |
| 1 | 1 | 0 |
| 0 | 0 | 1 |
| 0 | 1 | 0 |

|  |  |  |
| --- | --- | --- |
| Q1 | Q4 | Q |
| 1 | 0 | 0 |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 0 | 0 | 1 |

- Develop neuron and print truth table of XOR gate using only NAND gates



= [ A NAND ( A NAND B ) ] NAND

[ B NAND ( A NAND B ) ]

A B Q A Q1

0 0 1 0 1

0 1 1 0 1 Q1= [ A NAND ( A NAND B ) ]

1 0 1 1 0

1 1 0 1 1

A B Q B Q2

0 0 1 0 1

0 1 1 1 0 Q2= [ B NAND ( A NAND B ) ]

1 0 1 0 1

1 1 0 1 1

Q1 Q2 Q

1 1 0

1 0 1 = [ A NAND ( A NAND B ) ] NAND [ B NAND ( A NAND B ) ]

0 1 1

1 1 0